

90 (new). The memory cell, as set forth in claim 77, wherein the memory material comprises a programmable resistive element.

91 (new). The memory cell, as set forth in claim 90, wherein the programmable resistive element changes between different resistance levels in response to electrical stimulus.

REMARKS

At the time of the outstanding Official Action, claims 32-76 were pending, with claims 37, 40, 52, 55, 67, and 70 being objected to, and claims 32-36, 38, 39, 41-51, 53, 54, 56-66, 68, 69, and 71-76 being rejected. By this Amendment, independent claims 32 and 47 have been amended, and new claims 77-91 have been added. Reconsideration of the application as amended is respectfully requested.

In Applicants' Amendment mailed on February 27, 2002 in response to the Official Action dated November 27, 2001, Applicants presented arguments that the cited combination does not disclose or suggest, *inter alia*, an X-point memory cell. In the outstanding Official Action, the Examiner repeated the rejections and responded to Applicants' arguments by stating that: "it is noted that the features upon which applicant relies (i.e., where the access device is wholly disposed in the area of intersection of the digit line 26 and the word line 33 or where the chalcogenide memory element is wholly disposed in the area of intersection) are not recited in the rejected claim(s)."

Although the Examiner correctly noted that claims 32-66 did not specifically recite this general subject matter, claims 67-76 did recite this general subject matter. Thus, it appears that the Examiner did not give Applicants' arguments the necessary weight due to this oversight. By this Amendment, independent claims 32 and 47 have been amended and new claims 77-91 have been added to recite this general subject matter. Therefore, each of the pending claims 32-91 includes recitations that the access device and/or the memory element are wholly disposed in the area of intersection of the two lines. Accordingly, Applicants respectfully submit that all pending claims are patentable over the prior art of record for the reasons previously provided, and Applicants respectfully request withdrawal of all outstanding rejections and allowance of claims 32-91.

If the Examiner believes that a telephonic interview will help speed this application toward issuance, Applicants invite the Examiner to contact the undersigned at (281) 970-4545.

Attachment

Attached hereto is a clean version of the changes made to the claims by the current amendment. The attached page is captioned "**CLEAN VERSION TO SHOW CHANGES MADE.**"

General Authorization for Extensions of Time

In accordance with 37 C.F.R. § 1.136, Applicants hereby provide a general authorization to treat this and any future reply requiring an extension of time as incorporating a request therefor. Furthermore, Applicants authorize the Commissioner to charge the appropriate fee for any extension of time to Deposit Account No. 13-3092; Order No. MCRO:106--2/FLE (95-0412.02).

Respectfully submitted,

Date: August 21, 2002



Michael G. Fletcher
Reg. No. 32,777
FLETCHER, YODER & VAN SOMEREN
P.O. Box 692289
Houston, Texas 77269-2289
(281) 970-4545

CLEAN VERSION TO SHOW CHANGES MADE

IN THE CLAIMS

Please amend claims 32 and 47 as set forth below:

32. A memory cell comprising:

an area defined by an intersection of a word line and a bit line;

C
an access device;

a memory element operatively coupled to the access device, the memory element comprising:

dielectric material having a pore therein, the pore being smaller than a photolithographic limit;

a first electrode disposed within the pore;

a memory material disposed over the first electrode; and

a second electrode disposed over to the memory material; and

wherein at least one of the access device and the memory element is disposed wholly in
C¹ the area.

47. A memory cell comprising:

an area defined by an intersection of a word line and a bit line;

C² an access device;

a memory element operatively coupled to the access device, the memory element comprising a memory material disposed between a first electrode and a second electrode; and

dielectric material having a pore therein, the pore being smaller than a photolithographic limit, wherein at least one of the first electrode, the memory material, and the second electrode is disposed within the pore; and

wherein at least one of the access device and the memory element is disposed wholly in
the area.

Please add new claims 77-91 as set forth below:

77. An X-point memory cell comprising:

a first conductive line extending in a first direction;

a second conductive line extending in a second direction different than the first direction,

the first conductive line and the second conductive line being spaced apart by a portion of a substrate, the second conductive line intersecting the first conductive line in an overlapping manner to form an area of intersection in the portion of the substrate;

C³

an access device wholly disposed in the area of intersection, the access device being operatively coupled to one of the first conductive line and the second conductive line; and

a memory element wholly disposed in the area of intersection, the memory element being operatively coupled to the access device, the memory element comprising a memory material disposed between a first electrode and a second electrode.

78. The memory cell, as set forth in claim 77, wherein the access device comprises a diode.

79. The memory cell, as set forth in claim 78, wherein the diode comprises:

a layer of N doped polysilicon disposed adjacent a layer of P doped polysilicon.

80. The memory cell, as set forth in claim 77, wherein the first electrode is comprised of a plurality of layers.

81. The memory cell, as set forth in claim 77, wherein the first electrode is comprised of a plurality of materials.

*C³
C₆₀*

82. The memory cell, as set forth in claim 77, wherein the first electrode comprises:

a layer of carbon; and

a layer of titanium nitride disposed adjacent the layer of carbon.

83. The memory cell, as set forth in claim 77, wherein the second electrode is comprised of a plurality of layers.

84. The memory cell, as set forth in claim 77, wherein the second electrode is comprised of a plurality of materials.

85. The memory cell, as set forth in claim 77, wherein the second electrode comprises:

a layer of carbon; and

a layer of titanium nitride disposed adjacent the layer of carbon.

*C³
Cont.*

86. The memory cell, as set forth in claim 77, wherein the memory material comprises structure changing material.

87. The memory cell, as set forth in claim 86, wherein the structure changing material comprises a material which changes between different states of crystallinity in response to electrical stimulus.

88. The memory cell, as set forth in claim 87, wherein each of the different states of crystallinity corresponds to a given resistance level.

89. The memory cell, as set forth in claim 77, wherein the memory material comprises a chalcogenide material.

90. The memory cell, as set forth in claim 77, wherein the memory material comprises a programmable resistive element.

C³

91. The memory cell, as set forth in claim 90, wherein the programmable resistive element changes between different resistance levels in response to electrical stimulus.
